Amendments to the Claims

This listing will replace all prior versions, and listing, of claims in the application.

1. (currently amended) A method for creation of an interconnect pattern, comprising:

providing a layer of conductive material over a semiconductor surface, a layer of Anti Reflective Coating (ARC) having been deposited over the layer of conductive material;

depositing a layer of Photo-Active Dielectric (PAD) over the layer of ARC;

applying a direct patterned exposure to the layer of PAD, said direct patterned exposure comprising a patterned exposure without interposition of a patterned layer of photoresist serving as a photoresist mask between a source of exposure energy and the exposed layer of PAD, thereby patterning ~~and developing~~ the layer of PAD, creating an interconnect pattern therein, exposing the layer of ARC;

removing the exposed ARC; and

filling the interconnect pattern with a conductive material.

2. (original) The method of claim 1, wherein the conductive material comprises copper.

3. (currently amended) The method of claim 1, wherein the semiconductor surface is selected from the group consisting of a printed circuit board, a flex circuit, a metallized substrate, a glass substrate [[or]] and a semiconductor device mounting support.

4. (original) The method of claim 1, wherein the semiconductor surface is a semiconductor substrate.

5. (currently amended) The method of claim 4, wherein the semiconductor surface is selected from the group consisting of a ceramic substrate, a glass substrate, a gallium arsenide substrate, a silicon substrate comprising a single layer of material, such as a silicon wafer or comprising silicon on insulator (SOI) technology and silicon on sapphire (SOS) technology, a doped or undoped semiconductor, an epitaxial layer of silicon supported by a base semiconductor, a sapphire substrate [[or]] and a substrate used for flat panel displays.

6. (original) The method of claim 1, wherein the layer of Photo-Active Dielectric (PAD) is a polymer.

7. (currently amended) The method of claim 1, wherein the layer of Photo-Active Dielectric (PAD) is selected from the group consisting of a low-k polymer material including polyimides, fluorinated polyimides, polysilsequioxane, benzocyclobutene (BCB), parlene F, parlene N and amorphous polytetrafluorothylene.

8. (currently amended) The method of claim 1, wherein the layer of Photo-Active Dielectric (PAD) is selected from the group consisting of polycarbonate (PC), polystyrene (PS), polyoxides (PO), polymethylmethacrylate (PPMA) and poly-polyoxides (PPO).

9. (original) A method for creation of a dual damascene interconnect pattern, comprising:

providing a layer of conductive material over a semiconductor surface, a layer of Anti Reflective Coating (ARC) having been deposited over the layer of conductive material;

depositing a first layer of Photo-Active Dielectric (PAD) over the layer of ARC;

depositing a second layer of Photo-Active Dielectric over the first layer of Photo-Active Dielectric, the second layer of Photo-Active Dielectric comprising a Photo-Active Dielectric material having a different chemical composition than the first layer of Photo-Active Dielectric;

first patterning and developing the second layer of PAD, creating a trench pattern of a dual damascene pattern therein, exposing the first layer of PAD;

second patterning and developing the exposed first layer of PAD, creating a via pattern of a dual damascene pattern therein aligned with the trench pattern, the second patterning and developing comprising a different type of lithographic exposure than the first patterning and developing, exposing the layer of ARC;

removing the exposed ARC; and

filling the trench pattern and the via pattern with a conductive material.

10. (original) The method of claim 9, wherein the conductive material comprises copper.

11. (currently amended) The method of claim 9, wherein the semiconductor surface is selected from the group consisting of a

printed circuit board, a flex circuit, a metallized substrate, a glass substrate [[or]] and a semiconductor device mounting support.

12. (original) The method of claim 9, wherein the semiconductor surface is a semiconductor substrate.

13. (currently amended) The method of claim 12, wherein the semiconductor surface is selected from the group consisting of a ceramic substrate, a glass substrate, a gallium arsenide substrate, a silicon substrate comprising a single layer of material, such as a silicon wafer or comprising silicon on insulator (SOI) technology and silicon on sapphire (SOS) technology, a doped or undoped semiconductor, an epitaxial layer of silicon supported by a base semiconductor, a sapphire substrate [[or]] and a substrate used for flat panel displays.

14. (original) The method of claim 9, wherein the first layer of Photo-Active Dielectric (PAD) is a polymer.

15. (currently amended) The method of claim 9, wherein the first layer of Photo-Active Dielectric (PAD) is selected from the group consisting of a low-k polymer material including

polyimides, fluorinated polyimides, polysilsequioxane, benzocyclobutene (BCB), parlene F, parlene N and amorphous polytetrafluorothylene.

16. (currently amended) The method of claim 9, wherein the first layer of Photo-Active Dielectric (PAD) is selected from the group consisting of polycarbonate (PC), polystyrene (PS), polyoxides (PO), polymethylmethacrylate (PPMA) and poly-polyoxides (PPO).

17. (original) The method of claim 9, wherein the second layer of Photo-Active Dielectric (PAD) is a polymer.

18. (currently amended) The method of claim 9, wherein the second layer of Photo-Active Dielectric (PAD) is selected from the group consisting of a low-k polymer material including polyimides, fluorinated polyimides, polysilsequioxane, benzocyclobutene (BCB), parlene F, parlene N and amorphous polytetrafluorothylene.

19. (currently amended) The method of claim 9, wherein the second layer of Photo-Active Dielectric (PAD) is selected from the group consisting of polycarbonate (PC), polystyrene (PS),

polyoxides (PO), polymethylmethacrylate (PPMA) and poly-polyoxides (PPO).

20. (currently amended) The method of claim 9, wherein the different type of lithographic exposure is selected from the group consisting of UV lithography, DUV lithography, E-beam lithography, X-ray lithography [[or]] and ion beam lithography.

21. (original) The method of claim 9, wherein filling the trench pattern and the via pattern with a conductive material comprises methods of metal deposition followed by Chemical Mechanical Polishing (CMP).

22. (original) A method for creation of a dual damascene interconnect pattern, comprising:

providing a layer of conductive material over a semiconductor surface, a first layer of Anti Reflective Coating (ARC) having been deposited over the layer of conductive material;

depositing a first layer of Photo-Active Dielectric (PAD) over the first layer of ARC;

depositing a second layer of ARC over the first layer of PAD;

depositing a second layer of Photo-Active Dielectric over the second layer of ARC, the second layer of Photo-Active Dielectric comprising a Photo-Active Dielectric material having a different chemical composition than the first layer of Photo-Active Dielectric;

first patterning and developing the second layer of PAD, creating an trench pattern of a dual damascene pattern therein, exposing the second layer of ARC;

removing the exposed second layer of ARC, exposing the first layer of PAD;

second patterning and developing the first layer of PAD, creating a via pattern of a dual damascene pattern therein aligned with the trench pattern, the second patterning and developing comprising a different type of lithographic exposure than the first patterning and developing, exposing the first layer of ARC;

removing the exposed first layer of ARC; and

filling the trench pattern and the via pattern with a conductive material.

23. (original) The method of claim 22, wherein the conductive material comprises copper.

24. (currently amended) The method of claim 22, wherein the semiconductor surface is selected from the group consisting of a printed circuit board, a flex circuit, a metallized substrate, a glass substrate [[or]] and a semiconductor device mounting support.

25. (original) The method of claim 22, wherein the semiconductor surface is a semiconductor substrate.

26. (currently amended) The method of claim 25, wherein the semiconductor surface is selected from the group consisting of a ceramic substrate, a glass substrate, a gallium arsenide substrate, a silicon substrate comprising a single layer of material, such as a silicon wafer or comprising silicon on insulator (SOI) technology and silicon on sapphire (SOS) technology, a doped or undoped semiconductor, an epitaxial layer of silicon supported by a base semiconductor, a sapphire substrate [[or]] and a substrate used for flat panel displays.

27. (original) The method of claim 22, wherein the first layer of Photo-Active Dielectric (PAD) is a polymer.

28. (currently amended) The method of claim 22, wherein the first layer of Photo-Active Dielectric (PAD) is selected from the group consisting of a low-k polymer material including polyimides, fluorinated polyimides, polysilsequioxane, benzocyclobutene (BCB), parlene F, parlene N and amorphous polytetrafluorothylene.

29. (currently amended) The method of claim 22, wherein the first layer of Photo-Active Dielectric (PAD) is selected from the group consisting of polycarbonate (PC), polystyrene (PS), polyoxides (PO), polymethylmethacrylate (PPMA) and poly-polyoxides (PPO).

30. (original) The method of claim 22, wherein the second layer of Photo-Active Dielectric (PAD) is a polymer.

31. (currently amended) The method of claim 22, wherein the second layer of Photo-Active Dielectric (PAD) is selected from the group consisting of a low-k polymer material including polyimides, fluorinated polyimides, polysilsequioxane, benzocyclobutene (BCB), parlene F, parlene N and amorphous polytetrafluorothylene.

32. (currently amended) The method of claim 22, wherein the second layer of Photo-Active Dielectric (PAD) is selected from the group consisting of polycarbonate (PC), polystyrene (PS), polyoxides (PO), polymethylmethacrylate (PPMA) and poly-polyoxides (PPO).

33. (currently amended) The method of claim 22, wherein the different type of lithographic exposure is selected from the group consisting of UV exposure, DUV exposure, E-beam lithography, X-ray lithography [[or]] and ion beam lithography.

34. (original) The method of claim 22, wherein filling the trench pattern and the via pattern with a conductive material comprises methods of metal deposition followed by Chemical Mechanical Polishing (CMP).

Claims 35- 64: (cancelled).